UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/628,306	07/28/2000	Morishige Kinjo	04329.2354	3268

22852 7590 09/25/2003

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
1300 I STREET, NW
WASHINGTON, DC 20005

EXAMINER
ORTIZ, XIOMARA Y

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 09/25/2003

3

Please find below and/or attached an Office communication concerning this application or proceeding.

3

Office Action Summary	Application No.	Applicant(s)	
	09/628,306	KINJO ET AL.	
	Examiner	Art Unit	
	Xiomara Y. Ortiz	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☒ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because the abstract in an application filed should be limited to a paragraph within the range of 50 to 150 words. The abstract should be brief and contain the technical disclosure in the specification; it must commence on a separate sheet and preferably following the claims under the heading "Abstract of the Disclosure". Correction is required. See MPEP § 608.01(b).

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1,2,3,4,5,6,7,8,9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumasawa et al. U.S Patent No. 6,101,574 in view of Sherman, David L. U.S. Patent No. 6,141,765.

Regarding claim1, Kumasawa et al. discloses two systems that transfer instructions and data between each other. The two systems are link together by two paths, first, through a bridge that connects the internal buses of the systems so that data an instructions can be transmitted and received, and, second, through the channel buses that connects the two hosts computer with the two systems. The first and second systems comprise a duplex disk control unit whose each disk controller incorporates an MPU, a cache memory, an internal bus, and a controller to control disk units. The MPUs are connected to the internal bus which at the same time is connected through said bridge to the other internal bus to allow communication between the MPUs and copy the data from one cache memory to the other. However Kumasawa et al., fails to disclose that the first communication path which is used for information communication when a transfer size between the first system and the second system is smaller than a predetermined size and is capable of high-speed response when the transfer size is smaller than the predetermined size; and the second communication path which is used for information communication when the transfer size between the first system and the second system is larger than the predetermined size and has a larger transfer capability than that of said first communication path when the transfer size is larger than the predetermined size, wherein each of the first and second systems comprises main control means for controlling to selectively use one of said first and second communication paths in accordance with a size of information subjected to information communication with a counterpart system.

In addition, Sherman discloses, see fig.3, a router that would include a switch controller, a Gbridge circuit 78, a high-speed bus compatible dynamic random access memory (Gdram), 80, and a high-speed bus compatible content addressable memory (Gcam) 82. The switch controller and Gbridge would control the processing of the data packets entering and exiting the router as is well known. In the example, the second high-speed bus 76 would be divided into two separate buses, two separate data and address paths, 84 and 86,in order to provide two separate data and address path to the Gdram 80 and Gcam 82. In the router, the Gdram serves as a fast access, large size data packets, see col.12 line 58 to col.13 line 5. By definition, content addressable storage (Gcam), as also known associative storage, is used particularly in small, high-speed cache devices, see Microsoft Press Computer Dictionary second edition, page 29. It is implicit that the path to be used depends on the size of the data to be transfer in order to be stored. Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the above invention suggested by Kumasawa et al. and combining it with the invention disclosed by Sherman. One of ordinary skill in the art would have been motivated to do this combination in order to increase the internal operating speed of the information communication system, see col.13 lines 6-9.

Regarding claim 2, Kumasawa et al. in combination with Sherman, discloses all the limitations in claim 1. Kumasawa et al. also discloses internal buses 35-1 and 35-2 that are connected through a bridge circuit 144, that like an interface connects two elements so that they can work with one another. A system, communicates with the counterpart system through said first path so that instructions and data can be transmitted and received between MPUs 20-1 and

20-2, see col.7 lines 25-26. A system, communicates with the counterpart system through said second path so that the data on the cache that is updated by one disk control unit, is copied to the other disk control unit in order to guarantee that the cache data of the two disk control units are identical, see col.7 lines 30-33.

Regarding claim 3, Kumasawa et al. in combination with Sherman, discloses all the limitations in claim 2. Kumasawa et al. also discloses a third communication path for connecting the first and second systems, see fig. 2, and when a failure occurs on either first or second communication path, said third communication path may be used by the main control as an alternative path for the first or second path.

Regarding claim 4, Kumasawa et al. in combination with Sherman, discloses all the limitations in claim 2. Kumasawa et al. also discloses a system wherein the first and second systems comprise a duplex controller whose each controller incorporates a cache memory using a mirrored cache scheme, see fig. 2. When the data on the cache is updates by one disk control unit, the updated data is copied to the other disk control unit in order to guarantee that the cache data of the two-disk control unit are identical, col.7 lines 29-33.

Regarding claim5, Kumasawa et al. discloses two systems that transfer instructions and data between each other. However Kumasawa et al., fails to disclose a first communication path, used for communication between a first system and a second system; and a second communication path used for communication between the first system and the second system, wherein each of the first and second systems comprises means for determining one of said first

communication path and said second communication path, through which data is to be transferred, on the basis of a type of data to be exchanged between the first system and the second system.

In addition, Sherman discloses two separate data and address paths (84 and 86) to the Gdram 80 and Gcam 82, in which Gdram would serve as the fast access, large size data packets buffer for asynchronous transfer mode data packets, see col.13 lines 2-6, where it is clearly shown that the size of the data determines the data path to be used. Therefore at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the above invention suggested by Kumasawa et al. and combine it with the invention disclosed by Sherman. One of ordinary skill in the art would have been motivated to do this combination in order to increase the internal operating speed of the information communication system, see col.13 lines 6-9.

Regarding claim 6, Kumasawa et al. in combination with Sherman, discloses all the limitations in claim 5. Kumasawa et al. also discloses a system wherein the first and the second system are connected to six disk units 18-1 to 18-6 that are connected through a string controller 16 under the domination of the disk control 12, see fig.1, col.6 lines 49-51, and fig.2.

Regarding claim 7, Kumasawa et al. in combination with Sherman, discloses all the limitations in claim 6. Kumasawa et al. also discloses a system wherein the first and second systems comprise a cache memory 32 and a cache control unit 28 that executes a cache control for input/output request from host computers, see col.7 lines 4-8. The instructions and data can be transmitted and received between MPUs 20-1 and 20-2, see col.7 lines 23-26. As indicated

above in claim 5, (Sherman discloses two separate data and address paths (84 and 86) to the Gdram 80 and Gcam 82, in which Gdram would serve as the fast access, large size data packets buffer for asynchronous transfer mode data packets, see col.13 lines 2-6, where it is clearly shown that the size of the data determines the data path to be used.), the size of the transmission between MPUs and between cache memories defines the path to be use. Once it is determined that the first path is for small data transfer and the second path is for large data transfer, the corresponding transmission is performed. If the size of the transmission between MPUs is small, the first path is to be used, and if the transmission between the cache memories is large then the second path is to be used.

Regarding claim 8, Kumasawa et al. in combination with Sherman, discloses a system according to claim 5 wherein each of the fisrt and second system comprises internal buses 35-1 and 35-2 which connect disk control units 12-1 and 12-2. To perform communication with the counter part disk control unit through the first path, the disk control units 12-1 and 12-2 are connected through a bridge circuit 144, that like an interface connect two elements so they can work with one another, so that the instructions and data can be transmitted and received between MPUs 20-1 and 20-2, se col. 7 lines 23-26. To perform communication with the counter part disk control unit through the second path, the disk control units 12-1 and 12-2 are connected through a bridge circuit 144, that like an interface connect two elements so they can work with one another, and when the data on the cache is updated by one disk control unit, the updated data is copied to the other disk control unit in order to guarantee that the cache data of the two disk control unit are identical, see col.7 lines 30-33.

Regarding claim 9, Kumasawa et al. in combination with Sherman, discloses a system according to claim 8 that further comprises at least one disk control unit 12 of fig.1 with two systems, see col.7 lines 12-14, and a third path, 14-2 and 14-3 that connect the host computer to the counterpart system in the control unit 12, it may be used as an alternate path if one of the otrer two paths fails, see fig. 2.

Regarding claim 10, Kumasawa et al. in combination with Sherman, discloses a system, according to claim 8, whwrein the fisrt and secont systems comprise a duplex controller whose each controller incorporates a cache memory using a mirrored cache scheme, and a second path that when the data on the cache is updated by one this control unit, the updated data is copied to the other disk control unit in order to guarantee that the cache data of the two disk control units are identical, see col.7 lines 30-33.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to a communication system:

a. U.S. Pat. No. 5987569 to Tahashi et al., which discloses a memory control apparatus for controlling usage amounts for a plurality of cache memories.

b. U.S. Pat. No. 6029227 to Uchimura, which discloses a disk control apparatus to perform parallel data transfer from a plurality of disk devices.

c. U.S. Pat. No. 5574950 to Hathorn et al., which provides an improved design and method for communicating between host processors and storage controllers or between storage controllers.

d. U.S. Pat. No. 6145067 to Atsushi Kuwata, which discloses a disk array device with high-speed access to data and hard disk in parallel synchronously controlling them as one storage unit.

e. U.S. Pat. No. 5608891 to Mizuno et al., which discloses a recording system having a redundant array of storage devices and having read and write circuits with memory buffers.

f. U.S. Pat. No. 5579507 to Hosouchi et al., which discloses a data transfer control of virtual storage supported by three-level hierarchical storage.

g. U.S. Pat. No. 5652857 to Shimoi et al., which discloses a disk control apparatus for recording and reproducing compression data to physical device access type.

h. J.P.O. Pat. No. 11-298529 to Kinoshita, which discloses a communication path selection system, a communication path selection method, and a medium recording computer program to select a communication path.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiomara Y. Ortiz whose telephone number is (703) 305-6783. The examiner can normally be reached on Monday-Thursday from 8:30AM to 5:30PM. The examiner can also be reached on alternate Fridays. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on (703)

305-4003. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Xiomara Y. Ortiz
Patent Examiner
Art Unit 2141

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER